

NOTICE OF REVISION (NOR)				1. DATE (YYMMDD) 96-09-06		Form Approved OMB No. 0704-0188							
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.				Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.		2. PROCURING ACTIVITY NO.							
						3. DODAAC							
4. ORIGINATOR		b. ADDRESS (Street, City, State, Zip Code) Defense Supply Center, Columbus 3990 East Broad Street Columbus, OH 43216-5000		5. CAGE CODE 67268		6. NOR NO. 5962-R201-96							
a. TYPED NAME (First, Middle Initial, Last)				7. CAGE CODE 67268		8. DOCUMENT NO. 5962-92246							
9. TITLE OF DOCUMENT				10. REVISION LETTER		11. ECP NO.							
MICROCIRCUIT, DIGITAL, FAST CMOS, OCTAL TRANSCEIVER / REGISTER THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON				a. CURRENT A		N/A							
				b. NEW B									
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All													
13. DESCRIPTION OF REVISION													
Sheet 1: Revisions ltr column; add "B". Revisions description column; add "Changes in accordance with NOR 5962-R201-96". Revisions date column; add "96-09-06". Revision level block; change from "A" to "B". Rev status of sheets; for sheets 1 and 8, change from "A" to "B", and sheet 2, add "B". Sheet 2: 1.2.4, Case outline(s), Descriptive designator; change "GDIP1-T24 or CDIP2-T24" to "GDIP3-T24 or CDIP4-T24". Revision level block; add "B". Sheet 8: Table I, low level ground bounce noise, V_{OLV} , device types 01, 02 and 03; change maximum limit from "-1100" to "-1500". Revision level block; change from "A" to "B".													
14. THIS SECTION FOR GOVERNMENT USE ONLY													
a. (X one)		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50px; text-align: center;">X</td> <td>(1) Existing document supplemented by the NOR may be used in manufacture.</td> </tr> <tr> <td style="width: 50px;"></td> <td>(2) Revised document must be received before manufacturer may incorporate this change.</td> </tr> <tr> <td style="width: 50px;"></td> <td>(3) Custodian of master document shall make above revision and furnish revised document.</td> </tr> </table>						X	(1) Existing document supplemented by the NOR may be used in manufacture.		(2) Revised document must be received before manufacturer may incorporate this change.		(3) Custodian of master document shall make above revision and furnish revised document.
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b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT				c. TYPED NAME (First, Middle Initial, Last)									
DSCC-VAC				Monica L. Poelking									
d. TITLE		e. SIGNATURE			f. DATE SIGNED (YYMMDD)								
Chief, Custom Microelectronics		Monica L. Poelking			96-09-06								
15a. ACTIVITY ACCOMPLISHING REVISION		b. REVISION COMPLETED (Signature)			c. DATE SIGNED (YYMMDD)								
DSCC-VAC		Bernard J. Miesse			96-09-06								

NOTICE OF REVISION (NOR)				1. DATE (YYMMDD) 93-11-18		Form Approved OMB No. 0704-0188							
This revision described below has been authorized for the document listed.													
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						3. DODAAC							
4. ORIGINATOR		b. ADDRESS (Street, City, State, Zip Code) Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270		5. CAGE CODE 67268		6. NOR NO. 5962-R030-94							
a. TYPED NAME (First, Middle Initial, Last)				7. CAGE CODE 67268		8. DOCUMENT NO. 5962-92246							
9. TITLE OF DOCUMENT MICROCIRCUIT, DIGITAL, FAST CMOS, OCTAL TRANSCEIVER/REGISTER THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON				10. REVISION LETTER		11. ECP NO. N/A							
				a. CURRENT NEW				b. NEW A					
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES ALL													
13. DESCRIPTION OF REVISION Sheet 1: Revisions ltr column; add "A". Revisions description column; add "Changes in accordance with NOR 5962-R030-94". Revisions date column; add "93-11-18". Revision level block; add "A". Rev status of sheets; for sheets 1 and 8, add "A". Sheet 8: Table 1, off-state leakage current, I_{OFF} ; change maximum limit from "100 μA " for group A subgroups 1, 2, and 3 to "1.0 μA " for group A subgroups 1 and 2 and "5.0 μA " for group A subgroup 3. Revision level block; add "A".													
14. THIS SECTION FOR GOVERNMENT USE ONLY													
a. (X one)		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 5%; text-align: center;">X</td> <td>(1) Existing document supplemented by the NOR may be used in manufacture.</td> </tr> <tr> <td style="width: 5%;"></td> <td>(2) Revised document must be received before manufacturer may incorporate this change.</td> </tr> <tr> <td style="width: 5%;"></td> <td>(3) Custodian of master document shall make above revision and furnish revised document.</td> </tr> </table>						X	(1) Existing document supplemented by the NOR may be used in manufacture.		(2) Revised document must be received before manufacturer may incorporate this change.		(3) Custodian of master document shall make above revision and furnish revised document.
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b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECC				c. TYPED NAME (First, Middle Initial, Last) Monica L. Poelking									
d. TITLE Chief, Custom Microelectronics		e. SIGNATURE Monica L. Poelking			f. DATE SIGNED (YYMMDD) 93-11-18								
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ECC		b. REVISION COMPLETED (Signature) Joseph A. Kerby			c. DATE SIGNED (YYMMDD) 93-11-18								

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
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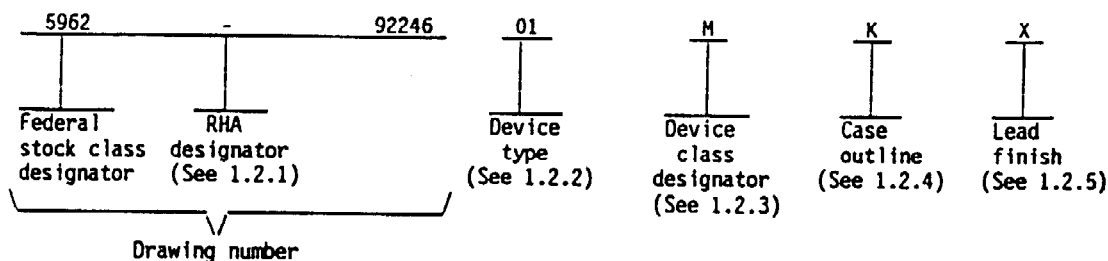
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PMIC N/A				PREPARED BY Joseph A. Kerby				DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																							
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Thomas J. Ricciuti				MICROCIRCUIT, DIGITAL, FAST CMOS OCTAL TRANSCEIVER/REGISTER, THREE- STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON																							
				APPROVED BY Monica L. Poelking																											
				DRAWING APPROVAL DATE 93-07-02																											
				REVISION LEVEL				SIZE A		CAGE CODE 67268		5962-92246																			
				SHEET 1 OF 22																											

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01, 04	54FCT652T	Octal transceiver/register, with three-state outputs, TTL compatible inputs and limited output voltage swing.
02, 05	54FCT652AT	Octal transceiver/register, with three-state outputs, TTL compatible inputs and limited output voltage swing.
03, 06	54FCT652CT	Octal transceiver/register, with three-state outputs, TTL compatible inputs and limited output voltage swing.

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP1-T24 or CDIP2-T24	24	dual-in-line
3	CQCC1-N28	28	leadless-chip-carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	- - - - -	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC output voltage range (V_{OUT})	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC input clamp current (I_{IK}) ($V_{IN} = -0.5$ V)	- - - - -	-20 mA
DC output clamp current (I_{OK}) ($V_{OUT} = -0.5$ V and +7.0 V)	- - - - -	± 20 mA
DC output source current (I_{OH}) per output	- - - - -	-30 mA
DC output sink current (I_{OL}) per output	- - - - -	+70 mA
DC V_{CC} current (I_{CC})	- - - - -	± 260 mA
DC ground current (I_{GND})	- - - - -	+550 mA
Storage temperature range (T_{STG})	- - - - -	-65°C to +150°C
Case temperature under bias (T_{BIAS})	- - - - -	-65°C to +135°C
Maximum power dissipation (P_D)	- - - - -	500 mW
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC})	- - - - -	See MIL-STD-1835
Junction temperature (T_J)	- - - - -	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	- - - - -	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	- - - - -	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	- - - - -	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	- - - - -	0.8 V
Minimum high level input voltage (V_{IH})	- - - - -	2.0 V
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C
Maximum input rise and fall rate (t_r, t_f): (from $V_{IN} = 0.3$ V to 2.7 V, 2.7 V to 0.3 V)	- - - - -	5 ns/V
Maximum high level output current (I_{OH})	- - - - -	-12 mA
Maximum low level output current (I_{OL})	- - - - -	48 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	- - - - -	XX percent 5/
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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For $V_{CC} \approx 6.5$ V, the upper limit on the range is limited to 7.0 V.

5/ Values will be added when they become available.

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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

- MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 37 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

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TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V Unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V _{OH1} 4/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -300 μA	All	4.5 V	1,2,3	3.0	V _{CC} -0.5	V
	V _{OH2}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OH} = -12 mA	All	4.5 V	1,2,3	2.4	V _{CC} -0.5	
Low level output voltage 3007	V _{OL1} 4/	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 300 μA	All	4.5 V	1,2,3		0.20	V
	V _{OL2}	For all inputs affecting output under test V _{IN} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND I _{OL} = 48 mA	All	4.5 V	1,2,3		0.55	
Three-state output leakage current high 3021	I _{OZH} 5/ 6/	G _{BA} = G _{AB} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND	V _{OUT} = V _{CC}	01,02,03	5.5 V	1,2	1.0	μA
						3	10.0	
						1	0.1	
						2,3	2.0	
Three-state output leakage current low 3020	I _{OZL} 5/ 6/	G _{BA} = G _{AB} = V _{IH} or V _{IL} V _{IH} = 2.0 V V _{IL} = 0.8 V For all other inputs V _{IN} = V _{CC} or GND	V _{OUT} = V _{CC}	01,02,03	5.5 V	1,2	-1.0	μA
						3	-10.0	
						1	-0.1	
						2,3	-2.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V Unless otherwise specified		Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
							Min	Max	
Negative input clamp voltage 3022	V _{IC-}	For input under test I _{IN} = -18 mA		01,02,03	4.5 V	1,2,3		-1.2	V
		For input under test I _{IN} = -15 mA		04,05,06				-1.3	
Input current high 3010	I _{IH}	For input under test V _{IN} = V _{CC} For all other inputs V _{IN} = V _{CC} or GND	control inputs	01,02,03	5.5 V	1,2		1.0	μA
			I/O pins			3		5.0	
						1,2		2.0	
						3		15.0	
				control inputs		1,2		0.1	
			I/O pins			3		1.0	
						1,2		0.2	
						3		3.0	
Input current low 3010	I _{IL}	For input under test V _{IN} = GND For all other inputs V _{IN} = V _{CC} or GND		control inputs	01,02,03	5.5 V	1,2		-1.0
			I/O pins	3				-5.0	
				1,2				-2.0	
				3				-15.0	
				control inputs	1,2			-0.1	
			I/O pins		3			-1.0	
					1,2			-0.2	
					3			-3.0	
Input capacitance 3012	C _{IN} <u>2/</u>	See 4.4.1c T _C = +25°C		All	GND	4		10	pF
Input/output capacitance 3012	C _{I/O} <u>2/</u>	See 4.4.1c T _C = +25°C		All	GND	4		12	pF
Short circuit output current 3005	I _{OS} <u>8/</u>	For all inputs V _{IN} = V _{CC} or GND V _{OUT} = GND		All	5.5 V	1,2,3	-60	-225	mA
Dynamic Power supply current	I _{CCD} <u>4/ 9/</u>	Outputs open		All	5.5 V	4,5,6		0.25	mA/ MHz•Bit

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V Unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Quiescent supply current delta, TTL input levels 3005	I _{ICC} <u>10/</u>	For input under test V _{IN} = V _{CC} - 2.1 V For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1,2,3		2.0	mA
Off-state leakage current	I _{OFF} <u>11/</u>	For input or output under test V _{IN} or V _{OUT} = 4.5 V All other pins at 0.0 V	All	0.0 V	1,2,3		100	μA
Quiescent supply current output high 3005	I _{CCH}	GBA = GAB = GND For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1,2,3		1.5	mA
Quiescent supply current output low 3005	I _{CCL}	GBA = GAB = GND For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1,2,3		1.5	mA
Quiescent supply current output three-state 3005	I _{CCZ} <u>5/</u>	GBA = GAB = V _{CC} For all other inputs V _{IN} = V _{CC} or GND	All	5.5 V	1,2,3		1.5	mA
Total supply current	I _{CCT} <u>12/</u>	Outputs open, GBA = GAB = GND f _{CP} = 10 MHz 50% Duty cycle, One bit toggling f _i = 5 MHz, 50% Duty cycle, For nonswitching inputs V _{CC} = V _{CC} or GND	For switching inputs V _{IN} = V _{CC} or GND	All	5.5 V	4,5,6	4.0	mA
		Outputs open, <u>4/</u> GBA = GAB = GND f _{CP} = 10 MHz 50% Duty cycle, Eight bits toggling f _i = 5.0 MHz, 50% Duty cycle, For nonswitching inputs V _{IN} = V _{CC} or GND	For switching inputs V _{IN} = 3.4 V or GND			4,5,6	6.0	
			For switching inputs V _{IN} = 3.4 V or GND			4,5,6	12.8	
						4,5,6	21.8	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V Unless otherwise specified	Device type	V _{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Low level ground bounce noise	V _{OLP} 13/	V _{IH} = 3.0 V V _{IL} = 0.0 V T _A = +25 °C See figure 4	01,02, 03	5.0 V	4		2000	mV
			04,05, 06					
Low level ground bounce noise	V _{OLV} 13/		01,02, 03	5.0 V	4		-1200	mV
			04,05, 06					
High level V _{CC} bounce noise	V _{OHP} 13/		01,02, 03	5.0 V	4		1200	mV
			04,05, 06					
High level V _{CC} bounce noise	V _{OHV} 13/		01,02, 03	5.0 V	4		-750	mV
			04,05, 06					
Functional test	14/	V _{IL} = 0.8 V V _{IH} = 2.0 V Verify output V _O See 4.4.1d	A11	4.5 V	7,8	L	H	
		V _{IL} = 0.8 V V _{IH} = 2.0 V Verify output V _O See 4.4.1d	A11	5.5 V	7,8	L	H	
Propagation delay time, data to output, A _n to B _n , B _n to A _n 3003	t _{PHL} , t _{PLH} 15/	C _L = 50 pF minimum, R _L = 500Ω, See figure 5	01,04	4.5 V	9,10,11	2.0	11.0	ns
			02,05		9,10,11	2.0	7.7	
			03,06		9,10,11	1.5	6.0	
Propagation delay time, SBA to A _n , SAB to B _n 3003	t _{PHL} , t _{PLH} 15/	C _L = 50 pF minimum, R _L = 500Ω, See figure 5	01,04	4.5 V	9,10,11	2.0	12.0	ns
			02,05		9,10,11	2.0	8.4	
			03,06		9,10,11	1.5	7.0	
Propagation delay time, output enable, GBA to A _n , GAB to B _n 3003	t _{PZH} , t _{PZL} 15/	C _L = 50 pF minimum, R _L = 500Ω, See figure 5	01,04	4.5 V	9,10,11	2.0	15.0	ns
			02,05		9,10,11	2.0	10.5	
			03,06		9,10,11	1.5	8.9	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ Unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output disable, GBA to An, GAB to Bn 3003	t_{PHZ} , t_{PLZ} 15/	$C_L = 50\text{ pF}$ minimum, $R_L = 500\Omega$, See figure 5	01,04	4.5 V	9,10,11	2.0	11.0	ns
			02,05		9,10,11	2.0	7.7	
			03,06		9,10,11	1.5	7.7	
Propagation delay time, clock to output, CPBA to An, CPAB to Bn 3003	t_{PLH} , t_{PHL} 15/	$C_L = 50\text{ pF}$ minimum, $R_L = 500\Omega$, See figure 5	01,04	4.5 V	9,10,11	2.0	10.0	ns
			02,04		9,10,11	2.0	7.0	
			03,06		9,10,11	1.5	6.3	
Set-up time, data high and low, An to CPAB, Bn to CPBA	t_s 15/	$C_L = 50\text{ pF}$ minimum, $R_L = 500\Omega$, See figure 5	01,04	4.5 V	9,10,11	4.5		ns
			02,05		9,10,11	2.0		
			03,06		9,10,11	2.0		
Hold time, data high and low, An from CPAB, Bn from CPBA	t_h 15/	$C_L = 50\text{ pF}$ minimum, $R_L = 500\Omega$, See figure 5	01,04	4.5 V	9,10,11	2.0		ns
			02,05		9,10,11	1.5		
			03,06		9,10,11	1.5		
Clock pulse width high or low, CPAB, CPBA	t_w 15/	$C_L = 50\text{ pF}$ minimum, $R_L = 500\Omega$, See figure 5	01,04	4.5 V	9,10,11	6.0		ns
			02,05		9,10,11	5.0		
			03,06		9,10,11	5.0		

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values: The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I.

5/ Three-state output conditions are required.

6/ This test may be performed using $V_{IH} = 3.0\text{ V}$. When $V_{IH} = 3.0\text{ V}$ is used, the test is guaranteed for $V_{IH} = 2.0\text{ V}$. This test is guaranteed by the I_{IL} and I_{IH} tests.

7/ This test is required only for Group A testing, see 4.4.1 herein.

8/ Not more than one output should be shorted at a time. The duration of the short circuit test should not exceed one second.

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9/ I_{CCD} may be verified by the following equation:

$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_i N_i}$$

where I_{CCT} , I_{CC} (I_{CCL} or I_{CCH} in table I), and ΔI_{CC} shall be the measured values of these parameters, for the device under test, when tested as described in table I, herein. The values for D_H , N_T , f_{CP} , f_i , N_i shall be as listed in the test conditions column for I_{CCT} in table I, herein.

10/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method: the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

11/ For I_{OFF} testing, test each input and output.

12/ I_{CCT} is calculated as follows:

$$I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_i N_i)$$

where

I_{CC} = Quiescent supply current (any I_{CCL} or I_{CCH})

D_H = Duty cycle for TTL inputs at 3.4 V

N_T = Number of TTL inputs at 3.4 V

ΔI_{CC} = Quiescent supply current delta, TTL inputs at 3.4 V

I_{CCD} = Dynamic power supply current caused by an input transition pair (HLH or LHL)

f_{CP} = Clock frequency for registered devices ($f_{CP} = 0$ for nonregistered devices)

f_i = Input frequency

N_i = Number of inputs at f_i

13/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than .25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50 Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL} . V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH} .

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH} . V_{OLV} and V_{OLP} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL} .

For device types 04, 05 and 06, limits will be added when these device types become available from an approved source of supply.

14/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 1.5$ V, $L < 1.5$ V.

15/ AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. Minimum propagation delay time limits for $V_{CC} = 4.5$ V and 5.5 V are guaranteed if not tested to the limits specified in table I, herein. For ac tests, all paths must be tested.

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Device types	01,02,03,04,05,06	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CPAB	NC
2	SAB	CPAB
3	GAB	SAB
4	A1	GAB
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	GBA	B3
22	SBA	NC
23	CPBA	B2
24	V _{CC}	B1
25	---	GBA
26	---	SBA
27	---	CPBA
28	---	V _{CC}

Pin descriptions	
Terminal symbol	Description
GAB, $\overline{\text{GBA}}$	Output enable control inputs
SAB, SBA	Output data source select inputs
CPAB, CPBA	Clock pulse timing inputs
A _n (n = 1 to 8)	Data register A inputs Data register B outputs
B _n (n = 1 to 8)	Data register B inputs Data register A outputs

FIGURE 1. Terminal connections.

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Inputs						Data I/O		Function
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA	An	Bn	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	I	I	X	X	Input	Input	Store A and B data
X	H	I	H or L	X	X	Input	Unspecified 1/	Store A, hold B
H	H	I	I	X 2/	X	Input	Output	Store A in both registers
L	X	H or L	I	X	X	Unspecified 1/	Input	Hold A store B
L	L	I	I	X	X 2/	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

- 1/ The data output functions may be enabled or disabled by various signals at the GAB or $\overline{\text{GBA}}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- 2/ Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered to load both registers
- H = High voltage level
L = Low voltage level
X = Don't care
I = Low-to-high transition

FIGURE 2. Truth table.

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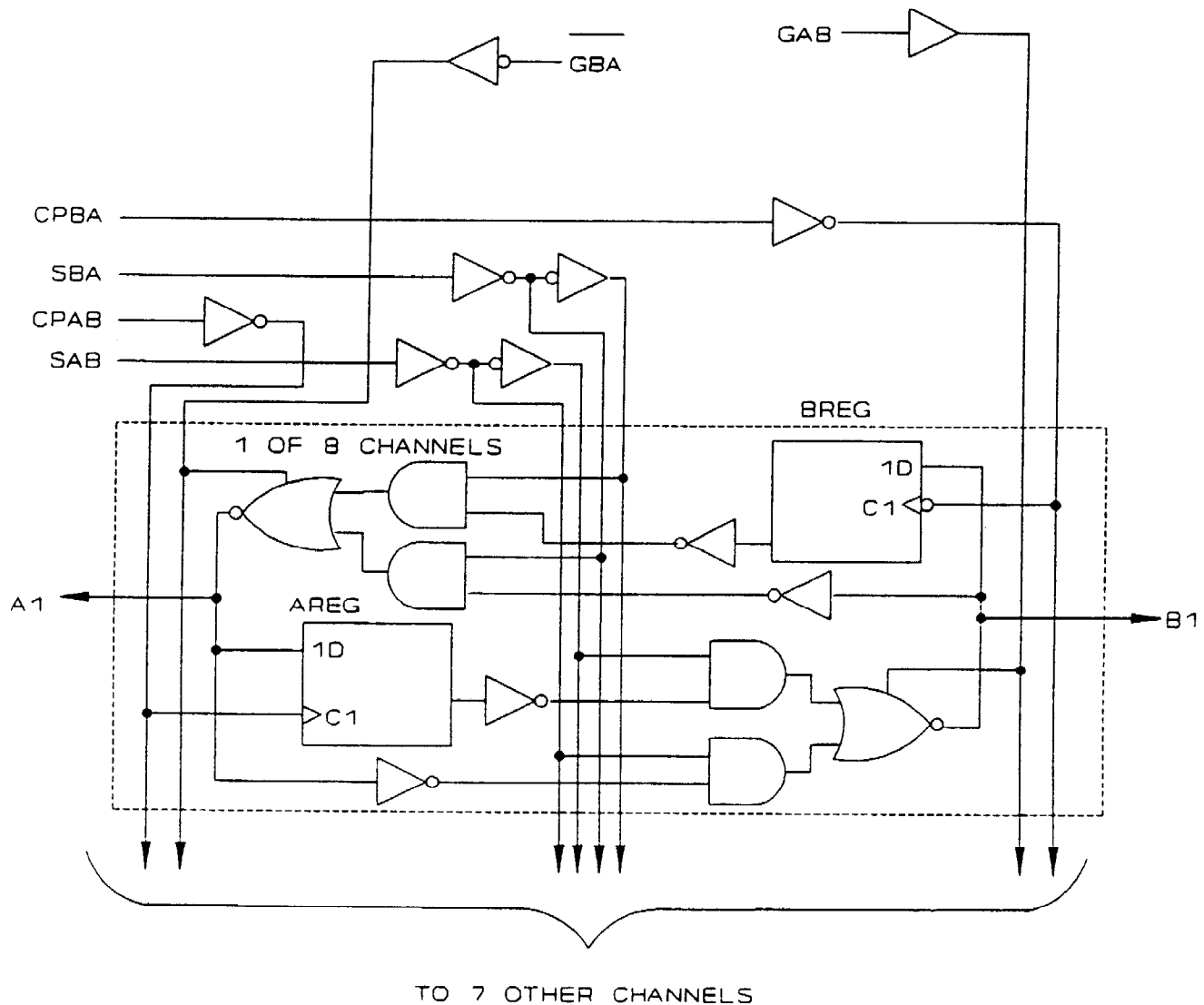


FIGURE 3. Logic diagram.

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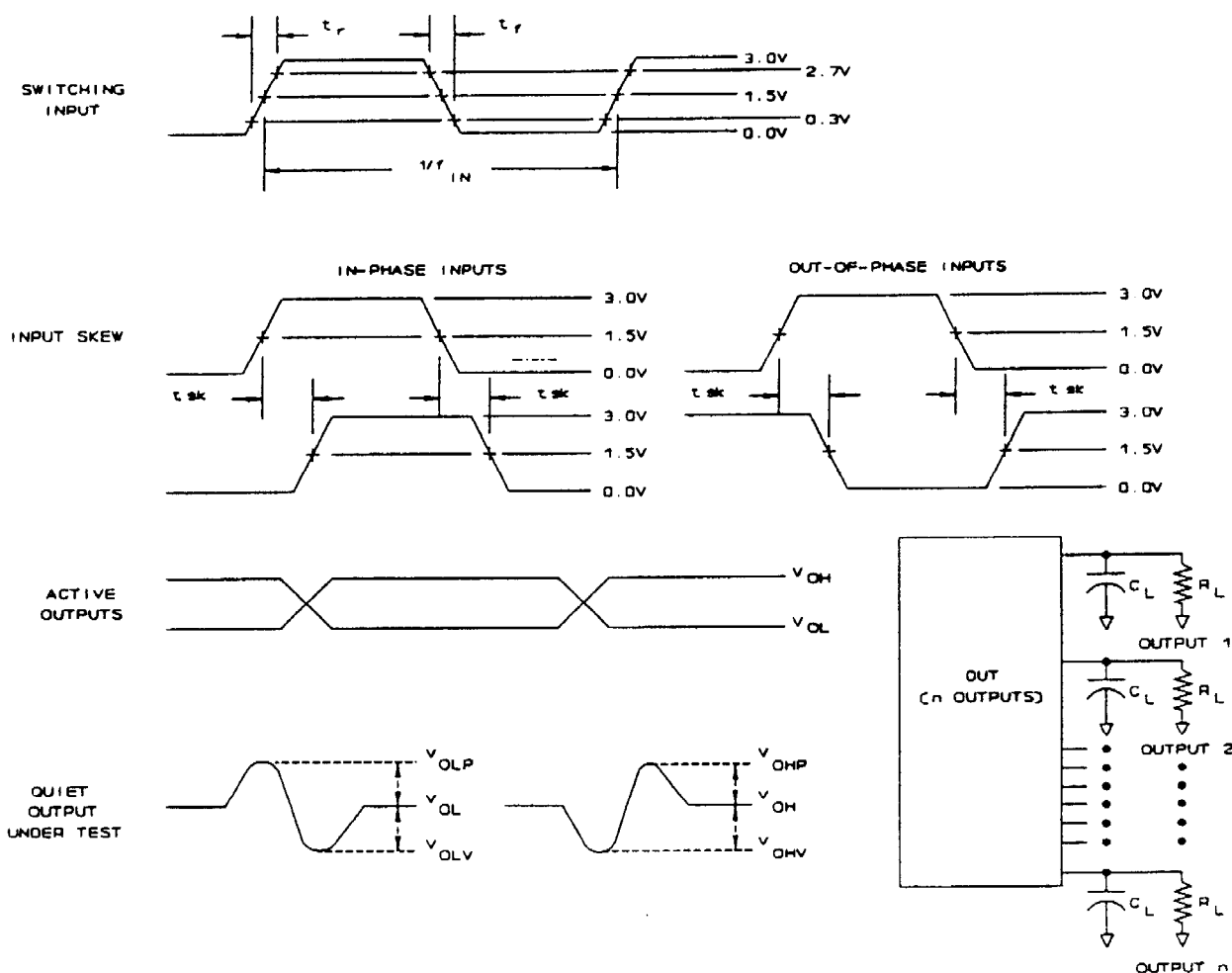
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NOTES:

C_L = 47 pF -0 percent, +20 percent chip capacitor plus ≥ 3 pF of equivalent capacitance from the test jig and probe.

R_L = 450 Ω ± 1 percent, chip resistor in series with a 50 Ω termination. For monitored outputs, the 50 Ω termination shall be the 50 Ω characteristic impedance of the coaxial connector to the oscilloscope.

Input signal to the device under test:

V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.

t_r , t_f = 3 ns ± 1.0 ns. For input signal generators incapable of maintaining this values of t_r and t_f , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ± 1.0 ns tolerance and guaranteeing the results at 3.0 ns ± 1.0 ns;

Skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 4. Ground bounce load circuit and waveforms.

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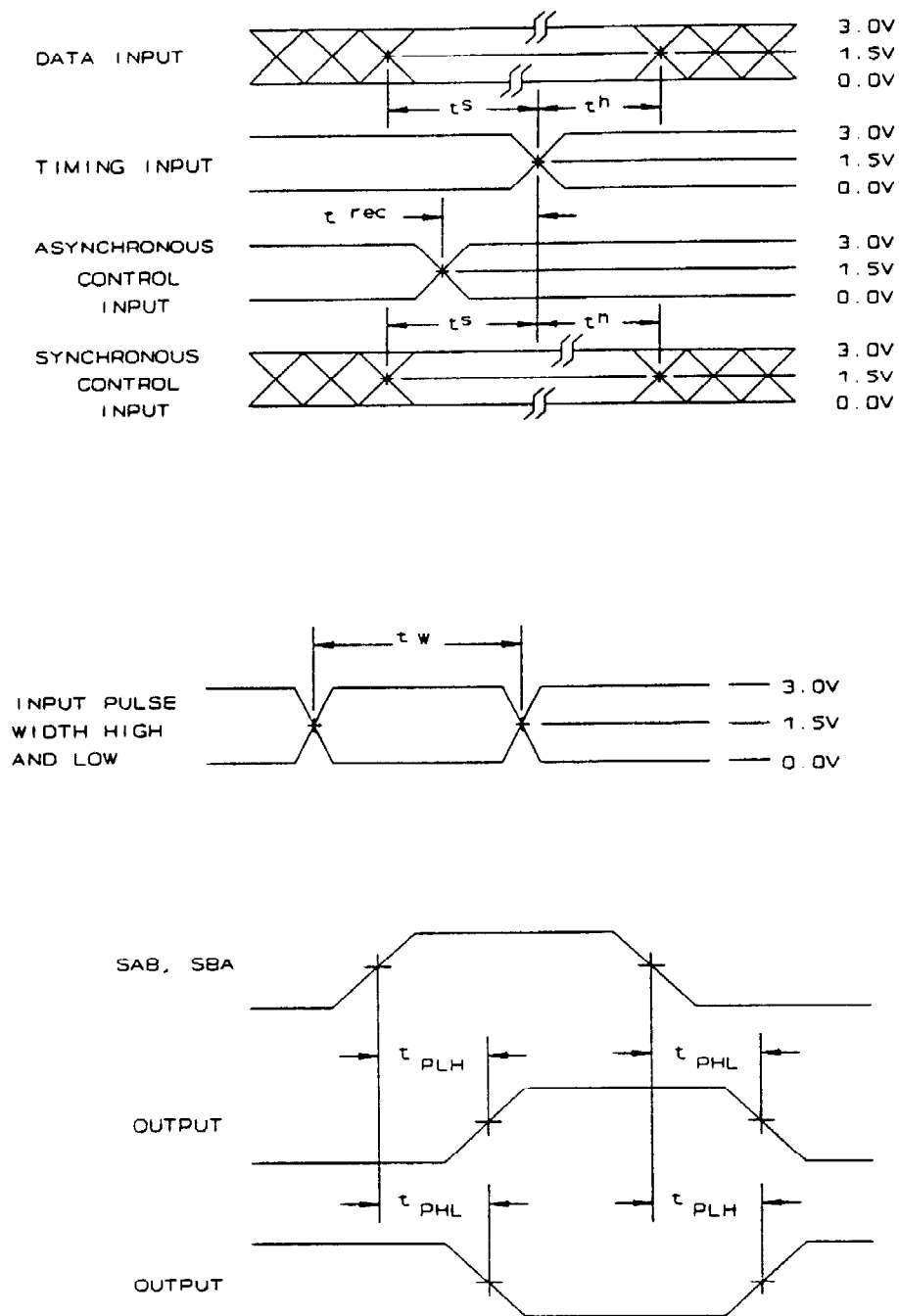


FIGURE 5. Switching waveforms and test circuit.

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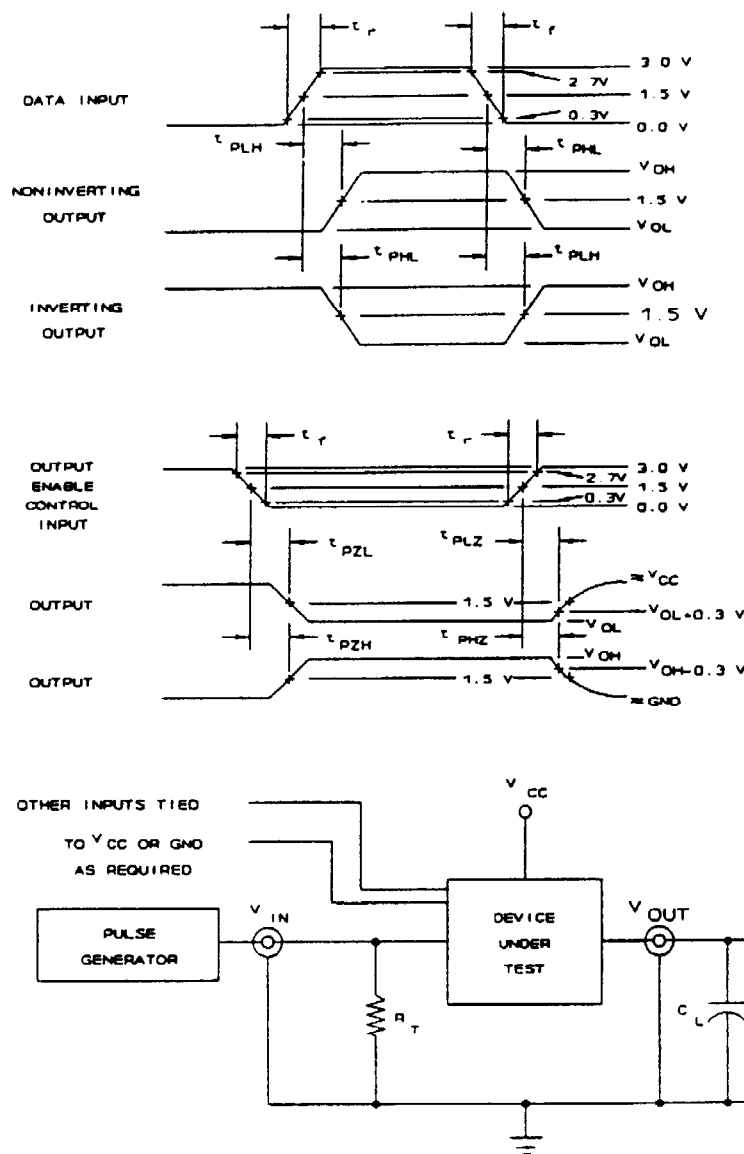
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NOTES:

When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 7.0 V$

When measuring t_{PHZ} , t_{PZH} , t_{PLH} and t_{PHL} : $V_{TEST} = \text{open}$

The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.

C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance)

R_L = 500 Ω or equivalent

R_T = 50 Ω or equivalent

Input signal from pulse generator: $V_{IN} = 0.0 V$ to $3.0 V$; $PRR \leq 10 \text{ MHz}$; duty cycle = 50 percent;

$t_r \leq 2.5 \text{ ns}$; $t_f \leq 2.5 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V, and 2.7 V to 0.3 V, respectively.

Timing parameters shall be tested at a minimum input frequency of 1 MHz.

The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device class B, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device class S, sampling and inspection procedures shall be in accordance with MIL-M-38510, and methods 5005 and 5007 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1	1	1
Final electrical parameters (see 4.2)	1/ 1,2,3, 4,5,6,7,8, 9,10,11	1/ 1,2,3, 4,5,6,7,8, 9,10,11	2/ 1,2,3, 4,5,6,7, 8,9,10,11	1/ 1,2,3, 4,5,6,7,8, 9,10,11	2/ 1,2,3, 4,5,6,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8, 9,10,11	1,2,3,4, 5,6,7,8,9, 10,11	1,2,3,4, 5,6,7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,4, 7,8,9, 10,11		1,2,3,4,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4, 5,6	1,2,3,4, 5,6		1,2,3,4, 5,6	
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,4,7,9	1,4,7,9	1,4,7,9	1,4,7,9	1,4,7,9

1/ PDA applies to subgroups 1 and 4 (i.e., I_{CCT} only).

2/ PDA applies to subgroups 1, 4 and 7.

4.3.3 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

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4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested to limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested to limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include, all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures, that shall include, all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP} , V_{OLV} , V_{OHP} , and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test."

c. C_{IN} and $C_{I/O}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and $C_{I/O}$, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. Class S steady-state life (accelerated) shall be conducted using test condition D of method 1005 of MIL-STD-883. For device class S steady-state life tests, the test circuit shall be submitted to and approved by the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. $T_A = +125^{\circ}\text{C}$, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

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4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-M-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as specified in table I at $T_A = +25^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331, and as follows:

GND	-----	Ground zero voltage potential.
I _{CC}	-----	Quiescent supply current.
I _{IL}	-----	Input current low.
I _{IH}	-----	Input current high.
T _C	-----	Case temperature.
T _A	-----	Ambient temperature.
V _A	-----	Positive supply voltage.
C _{CC}	-----	Input terminal-to-GND capacitance.
V _{IC}	-----	Negative input clamp voltage.

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-07-02

Approved sources of supply for SMD 5962-92246 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9224601MLX	61772	IDT54FCT652TDB
5962-9224601MKX	61772	IDT54FCT652TEB
5962-9224601M3X	61772	IDT54FCT652TLB
5962-9224602MLX	61772	IDT54FCT652ATDB
5962-9224602MKX	61772	IDT54FCT652ATEB
5962-9224602M3X	61772	IDT54FCT652ATLB
5962-9224603MLX	61772	IDT54FCT652CTDB
5962-9224603MLX	61772	IDT54FCT652CTEB
5962-9224603M3X	61772	IDT54FCT652CTLB
5962-9224604MLX	2/	
5962-9224604M3X	2/	
5962-9224605MLX	2/	
5962-9224605M3X	2/	
5962-9224606MLX	2/	
5962-9224606M3X	2/	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply as of the date of this drawing.

Vendor CAGE
number
61772

Vendor name
and address
Integrated Devices Technology Inc.
3236 Scott Boulevard
P.O. Box 58015
Santa Clara, CA 95052

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.